AMENDMENTS TO THE CLAIMS

1-28. (Canceled)

29. (Currently amended) An implantable amplifying circuit for recording electrical signals generated by a nerve and detected by a pair of electrode wires in contact with the nerve, the amplifying circuit comprising:

a preamplifier having a pair of inputs for receiving signals from the pair of electrode wires, the preamplifier including a differential pair of input MOSFET transistors having a low input current that serves as a first [[input]] protection circuit to limit current flow through the nerve and the electrode wires;

a common signal line that ~~is couplable to the nerve~~ connects a body ground of a patient to a common voltage of the amplifying circuit;

a second [[input]] protection circuit disposed in series with the common signal line including a parallel resistor/capacitor combination to limit current flow through the nerve and the common signal line.

30. (Previously presented) The implantable amplifying circuit of claim 29, wherein the preamplifier includes a pair of bipolar transistors and a current mirror that are driven with differential outputs of the MOSFET input transistors and produces a single-ended nerve output signal.

31. (Currently amended) The implantable amplifying circuit of claim 29, wherein said second [[input]] protection circuit comprises a resistor in parallel with a series of one or more capacitors~~, said parallel pair connected between the common signal line connectable to the nerve and a reference voltage terminal that provides a virtual ground terminal in respect of said implantable amplifying circuit~~.

32. (Previously presented) The implantable amplifying circuit of claim 29, further comprising:

at least one amplifier stage connected to an output at the preamplifier that produces an amplified nerve output signal.

33. (Previously presented) The implantable amplifying circuit of claim 32, further comprising a DC restoration circuit having an input connected to an output of said amplifier stage.

34. (Previously presented) The implantable amplifying circuit of claim 32, wherein said amplifier stage is a band-pass amplifier.

35. (Previously presented) The implantable amplifying circuit of claim 34, wherein said band-pass amplifier comprises a plurality of high-pass filters and a plurality of low-pass negative-feedback amplifiers alternatingly cascaded with said high-pass filters.

36. (Previously presented) The implantable amplifying circuit of claim 34, wherein said band-pass amplifier is a programmable-gain band-pass amplifier.

37. (Previously presented) The implantable amplifying circuit of claim 35, wherein each low-pass negative-feedback amplifier comprises:

a plurality of series-connected resistors forming a resistor string connected between an output terminal and a voltage reference terminal of the low-pass negative-feedback amplifier; and

a plurality of selectable switches wherein an end of each selectable switch is connected to an input terminal of the low-pass negative-feedback amplifier and another end of each selectable switch is connected to a nodal point between the resistors in the resistor string.

38. (Previously presented) The implantable amplifying circuit of claim 35, wherein each low-pass negative-feedback amplifier comprises an output stage in a Darlington

configuration operating as a class AB amplifier wherein a bias circuit supplying bias to the output stage also carries signal current.

39. (Previously presented) The implantable amplifying circuit of claim 36, wherein said programmable-gain band-pass amplifier has a frequency range between approximately 900 Hz and 9 kHz for 5 μV_{peak} input neural signals.

40. (Previously presented) The implantable amplifying circuit of claim 29, wherein the implantable amplifying circuit has an equivalent input noise at 3 kHz that is lower than 0.6 μV_{rms}.

41. (Previously presented) The implantable amplifying circuit of claim 29, wherein the implantable amplifying circuit has a CMRR higher than 90 dB at 250 Hz.

42. (Previously presented) The implantable amplifying circuit of claim 29, wherein the implantable amplifying circuit has a power consumption lower than 12 mW.

43. (Previously presented) The implantable amplifying circuit of claim 29, wherein the preamplifier has an input DC current that is lower than 1 nanoamp.

44. (Previously presented) The implantable amplifying circuit of claim 29, wherein said implantable amplifying circuit is powered by an RF telemetry link.

45. (Previously presented) The implantable amplifying circuit of claim 29, wherein the implantable amplifying circuit has a PSRR higher than 85 dB at 3 kHz.

46. (Previously presented) The implantable amplifying circuit of claim 29, wherein said implantable amplifying circuit is powered by a battery.